

WHAT IS CLAIMED IS:

- 1 1. A device comprising:
2 a package module having a footprint size based on a standard package;
3 an unpackaged semiconductor die directly attached to the package module; and
4 a packaged semiconductor attached to the multi-die module.
- 1 2. The device as in Claim 1, wherein the packaged semiconductor is packaged in a ball grid
2 array package.
- 1 3. The device as in Claim 1, wherein the unpackaged semiconductor die is a graphics-processor.
- 1 4. The device as in Claim 1, wherein the packaged semiconductor is a memory.
- 1 5. The device as in Claim 1, wherein a plurality of packaged semiconductors are attached to the
2 multi-die module.
- 1 6. The device as in Claim 1, wherein directly attached includes wire bonded.
- 1 7. The device as in Claim 1, wherein directly attached includes flip-chip attachment.
- 1 8. The device as in Claim 1, wherein attached includes surface-mount technology reflow.
- 1 9. The device as in Claim 1, wherein the unpackaged semiconductor die is encapsulated.
- 1 10. The device as in Claim 1, wherein the unpackaged semiconductor die is underfilled.

- 1 11. The device as in Claim 1, wherein the footprint size of the package module is one of 35mm
2 X 35mm, 31mm X 31mm, 27mm X 27mm, 37.5mm X 37.5mm, 40mm X 40mm, 42mm X
3 42mm, or 42.5mm X 42.5mm.
- 1 12. The device as in Claim 1, further including a heat sink.
- 1 13. The device as in Claim 12, wherein a top surface of the unpackaged semiconductor die and a
2 top surface of the packaged semiconductor are of substantially equal distance from a surface
3 of the package module.
- 1 14. The device as in Claim 12, further including a shim positioned over the unpackaged
2 semiconductor die such that a top of the shim and a top surface of the packaged
3 semiconductor are of substantially equal distance from a surface of the multi-die module.

- 1 15. A device comprising:
2 a package module sized to be interchangeable with standard package sizes;
3 a graphics-processing die directly attached to the package module; and
4 a packaged memory attached to the package module.
- 1 16. The device as in Claim 15, wherein the packaged memory is packaged in a ball grid array
2 package.
- 1 17. The device as in Claim 15, wherein a plurality of packaged memory are attached to the multi-
2 die module.
- 1 18. The device as in Claim 15, wherein directly attached includes wire bonded.
- 1 19. The device as in Claim 15, wherein directly attached includes flip-chip attachment.
- 1 20. The device as in Claim 15, wherein attached includes surface-mount technology reflow.
- 1 21. The device as in Claim 15, wherein the graphics-processing die is encapsulated.
- 1 22. The device as in Claim 15, wherein the graphics-processing die is underfilled.
- 1 23. The device as in Claim 15, wherein the standard package sizes include one of 35mm X
2 35mm, 31mm X 31mm, 27mm X 27mm, 37.5mm X 37.5mm, 40mm X 40mm, 42mm X
3 42mm, or 42.5mm X 42.5mm.
- 1 24. The device as in Claim 15, further including a heat sink.

1 25. The device as in Claim 24, wherein a top surface of the graphics-processor die and a top
2 surface of the packaged memory are of substantially equal distance from a surface of the
3 package module.

1 26. The device as in Claim 24, further including a shim positioned on top of the graphics-
2 processor die such that a top of the shim and a top surface of the packaged memory are of
3 substantially equal distance from a surface of the package module.

- 1 27. A method comprising the steps of:
2 directly attaching a first semiconductor die to a package substrate;
3 forming electrical connections between the first semiconductor die and the package
4 substrate;
5 securing the electrical connections;
6 placing a second semiconductor die in a die package;
7 attaching the die package to the package substrate; and
8 forming electrical connections between the die package and the package substrate.
- 1 28. The method as in Claim 27, wherein the step of placing the second semiconductor die in a
2 die package includes placing the semiconductor die in a ball grid array package.
- 1 29. The method as in Claim 27, wherein the steps of directly attaching and forming electrical
2 connections are performed using a flip-chip process.
- 1 30. The method as in Claim 27, wherein the steps of attaching and forming electrical connections
2 are performed using surface mount technology reflow.
- 1 31. The method as in Claim 27, wherein the step of directly attaching includes the use of
2 adhesives.
- 1 32. The method as in Claim 27, wherein the steps of forming electrical connections include wire-
2 bonding.
- 1 33. The method as in Claim 27, wherein securing the electrical connections includes
2 encapsulating the first semiconductor die.

- 1 34. The method as in Claim 27, wherein securing the electrical connections includes underfilling
2 the first semiconductor die.
- 1 35. The method as in Claim 27, further including the step of attaching solder balls to an
2 underside of the package substrate.
- 1 36. The method as in Claim 27, wherein the package substrate has a footprint of one of 35mm X
2 35mm, 31mm X 31mm, 27mm X 27mm, 37.5mm X 37.5mm, 40mm X 40mm, 42mm X
3 42mm, or 42.5mm X 42.5mm.
- 1 37. The method as in Claim 27, further including the step of attaching a heat sink to the package
2 substrate.
- 1 38. The method as in Claim 37, further including the step of positioning a shim on top of the first
2 semiconductor die such that a top of the shim and a top surface of the die package are of
3 substantially equal distance from a surface of the package substrate.
- 1 39. The method as in Claim 27, further including the step of testing the first semiconductor die
2 prior to the step of attaching the die package to the package substrate.
- 1 40. The method as in Claim 27, further including the step of testing the second semiconductor
2 die after the step of placing the second semiconductor die in a die package and prior to the
3 step of attaching the die package.